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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,681	11/30/2001	Alain E. Perregaux	D/A1232	4178

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 01/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,681	PERREGAUX ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-20* is/are allowed.

6)☒ Claim(s) *1-9 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1203*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida (US 6,117,347)

Ishida discloses a method for separation wafers into individual dielectric comprises the steps of:

using plasma etching/dry etch to etch U-groove 21 in the semiconductor wafer (col 3, lines 49-51, fig. 1B)

sawing the semiconductor wafer along the groove 21 where one edge of the saw 30 is aligned with the bottom of groove 21 (col 3, lines 24-26, fig. 1C)

Regarding claim 3, Ishida discloses that silicon substrate can be used in his invention.

3. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Kashiwa et al (US 5,302,554)

Kashiwa discloses a method for producing semiconductor chip/device from a wafer. This method comprises the step of:

chemically etching small U-shaped grooves/dicing lines 2 in one side of wafer (col 3, lines 54-56), which reads on etching small U-shaped grooves in one side of a wafer delineating the faces of the dies where the dies are to be separated from the wafer

forming grooves 4 in the rear/opposite side of the wafer opposite each of U-shaped grooves 2, the axis of grooves 4 is parallel to the axis of the U-shaped groove 2 (col 3, lines 65-67, fig. 2(d))

cutting/sawing the wafer along the grooves 2 with one side of the cut made by the blade 6 being substantially coextensive with the bottom of groove 2 (fig. 3(a)), fig. 3(b) of Kashiwa shows that one side of groove 2 is obligated by the blade/saw 6 while a portion of the groove remains

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (US 6,117,347) in view of Bondur et al (US 4,726,879)

Ishida's method has been described above. Unlike the instant claimed invention as per claim 2, Ishida fails to disclose the step of dry etching using a combination of SF6 and oxygen.

However, Bondur discloses a method for dry etching trenches/groove in semiconductor substrate comprises the step of dry etching a trench using a combination of SF6 and oxygen (col 5, lines 31-33; col 6, lines 10-11)

Hence, one skilled in the art would have found it obvious to modify Ishida's step of dry etching the groove by dry etching using a combination of SF6 and oxygen as per Bondur because Bondur teaches that the gas mixture of SF6 and oxygen would facilitate a high etch rate ratio of semiconductor to insulator while providing excellent controllability of the etching process (col 5, lines 43-45)

6. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (US 6,117,347) in view of MacDonald, Jr et al (US 6,184,570))

Ishida's method has been described above. Unlike the instant claimed invention as per claims 4-6, Ishida does not specifically disclose that the semiconductor wafer is comprised of gallium arsenide/III-V compound, silicon on insulator.

MacDonald discloses a method for forming semiconductor dies comprises the step of forming semiconductor dies from gallium arsenide/III-V compound and silicon on insulator (col 4, lines 30-35)

Hence, one skilled in the art would have found it obvious to modify Ishida's method by forming the semiconductor substrate from gallium arsenide/III-V compound and silicon on insulator as per MacDonald because MacDonald states that the integrated dielectric may be fabricated of gallium arsenide or may include an active substrate including SOI substrate (col 4, lines 29-35)

7. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (US 6,117,347) in view of Sherrer et al (US 6,363,201)

Ishida's method has been described above. Unlike the instant claimed invention as per claims 7-9, Ishida fails to disclose the specific dimensions (depth and width) of the groove.

However, Sherrer discloses a method for forming semiconductor chip comprises the step of forming the wick stop trench 26 /U-shaped grooves in the range of 5 microns (col 3, lines 57-60)

Hence, one skilled in the art would have found it obvious to modify Ishida's method by forming the U-shaped trench/groove having the dimensions as taught per Sherrer because according to Sherrer a wick stop trench/U-shaped trench can have a wide range of depth and widths (col 3, lines 35-37)

8. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kashiwa et al (US 5,302,554) in view of Bondur et al (US 4,726,879)

Kashiwa's method has been described above. Unlike the instant claimed invention as per claim 22, Kashiwa fails to disclose the step of dry etching using a combination of SF6 and oxygen.

However, Bondur discloses a method for dry etching trenches/groove in semiconductor substrate comprises the step of dry etching a trench using a combination of SF6 and oxygen (col 5, lines 31-33; col 6, lines 10-11)

Hence, one skilled in the art would have found it obvious to modify Kashiwa's step of chemical etching the groove by dry etching using a combination of SF6 and oxygen as per Bondur because Bondur teaches that the gas mixture of SF6 and oxygen would facilitate a high etch rate ratio of semiconductor to insulator while providing excellent controllability of the etching process (col 5, lines 43-45)

9. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kashiwa et al (US 5,302,554) in view of Sherrer et al (US 6,363,201)

Kashiwa's method has been described above. Unlike the instant claimed invention as per claims 23-26, Kashiwa fails to disclose the specific dimensions (depth and width) of the groove.

However, Sherrer discloses a method for forming semiconductor chip comprises the step of forming the wick stop trench 26 /U-shaped grooves in the range of 5 microns (col 3, lines 57-60)

Hence, one skilled in the art would have found it obvious to modify Kashiwa's method by forming the U-shaped trench/groove having the dimensions as taught per Sherrer because according to Sherrer a wick stop trench/U-shaped trench can have a wide range of depth and widths (col 3, lines 35-37)

Allowable Subject Matter

10. Claims 10-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 10, the cited prior art of record fails to disclose a method for dicing die comprises the step of etching by way of a second dry etch a U-groove in the opening down to the surface of the semiconductor wafer created by the first dry etch. The closest cited prior art of Kosaki (US 5,998,238) discloses a method for fabricating semiconductor chip comprises the step of second wet etch a U-groove 2 in the opening down to the surface of the semiconductor wafer created by the first dry etch (col 25, lines 7-10)

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

LV
December 19, 2003